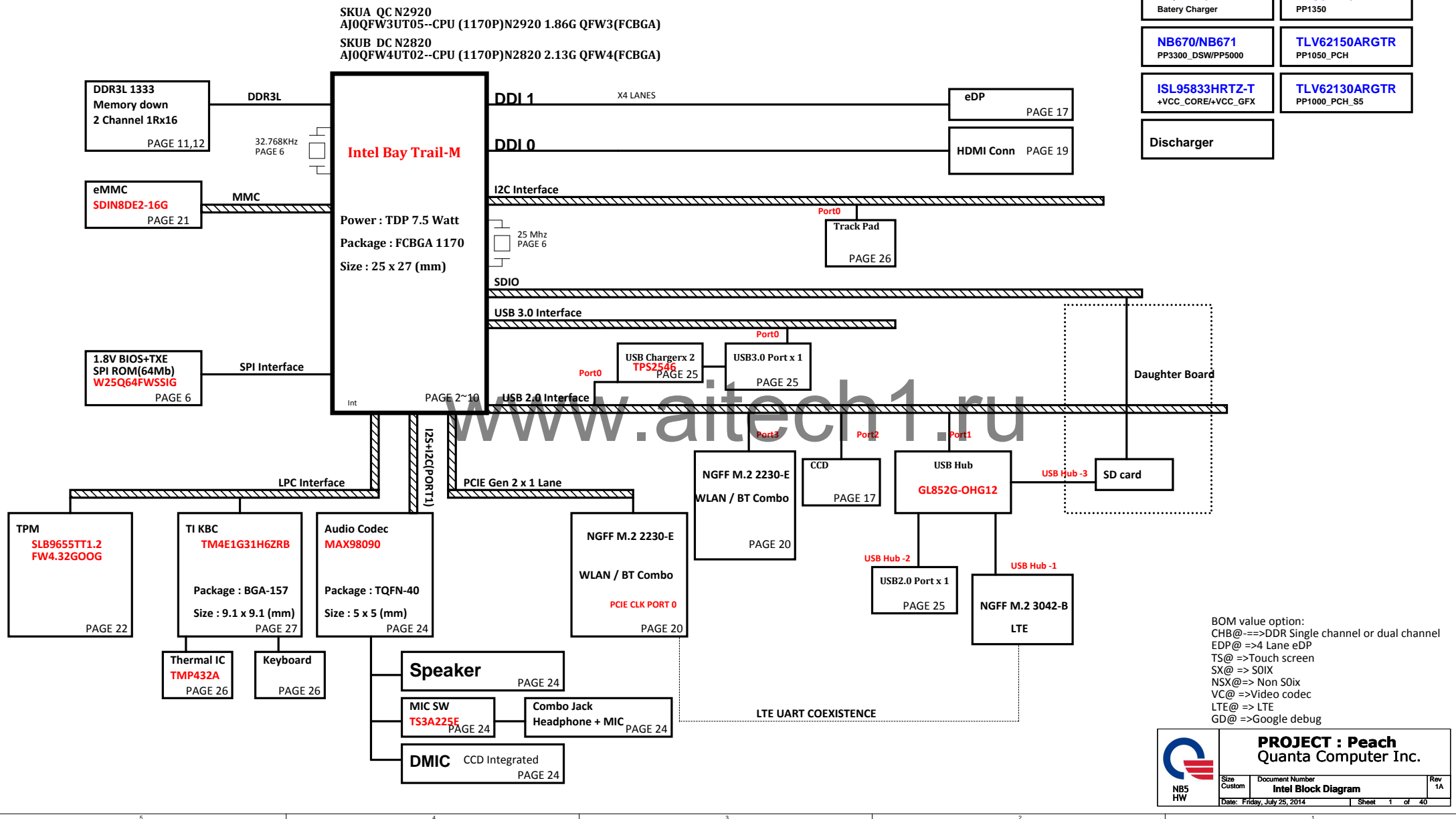
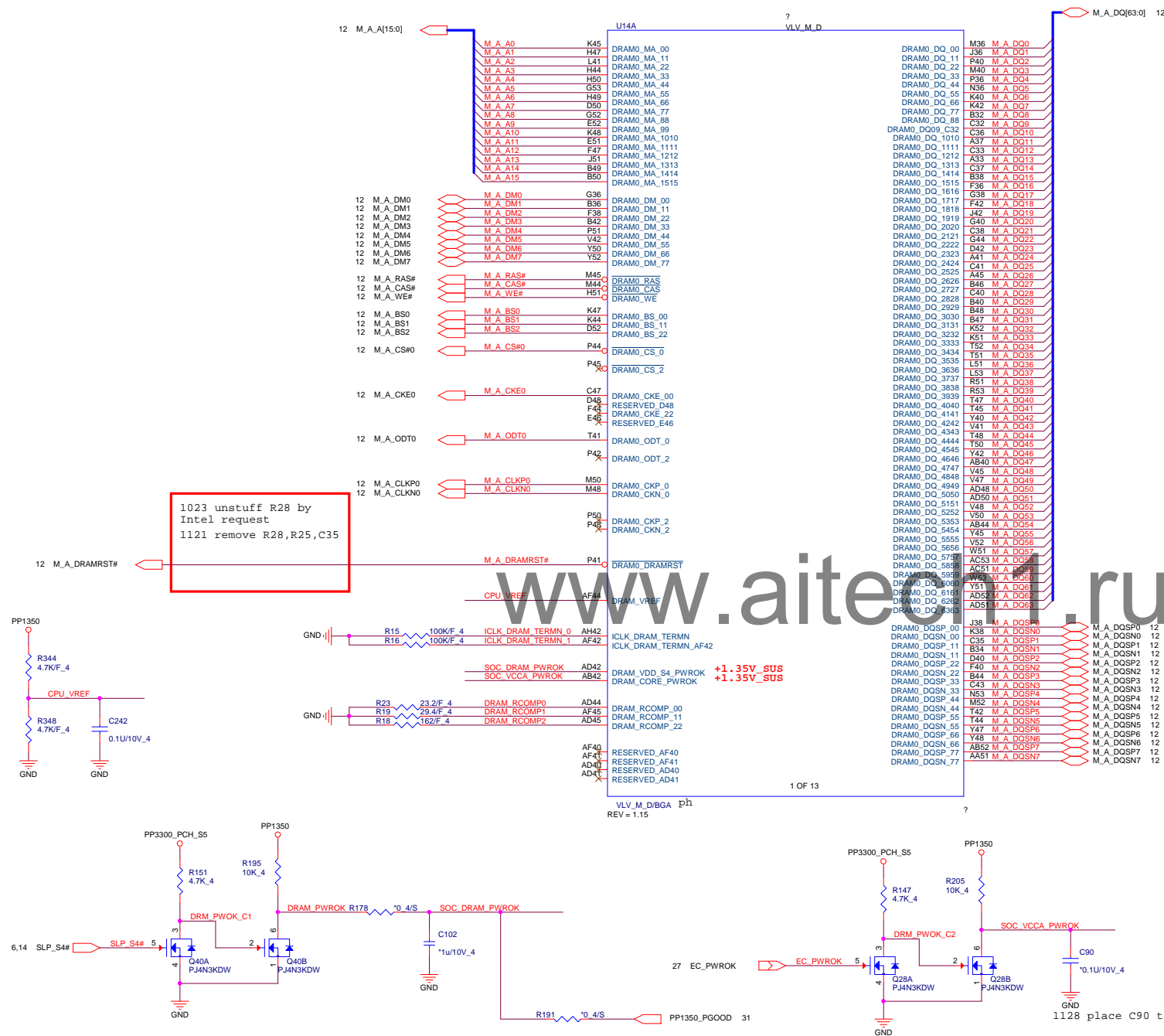


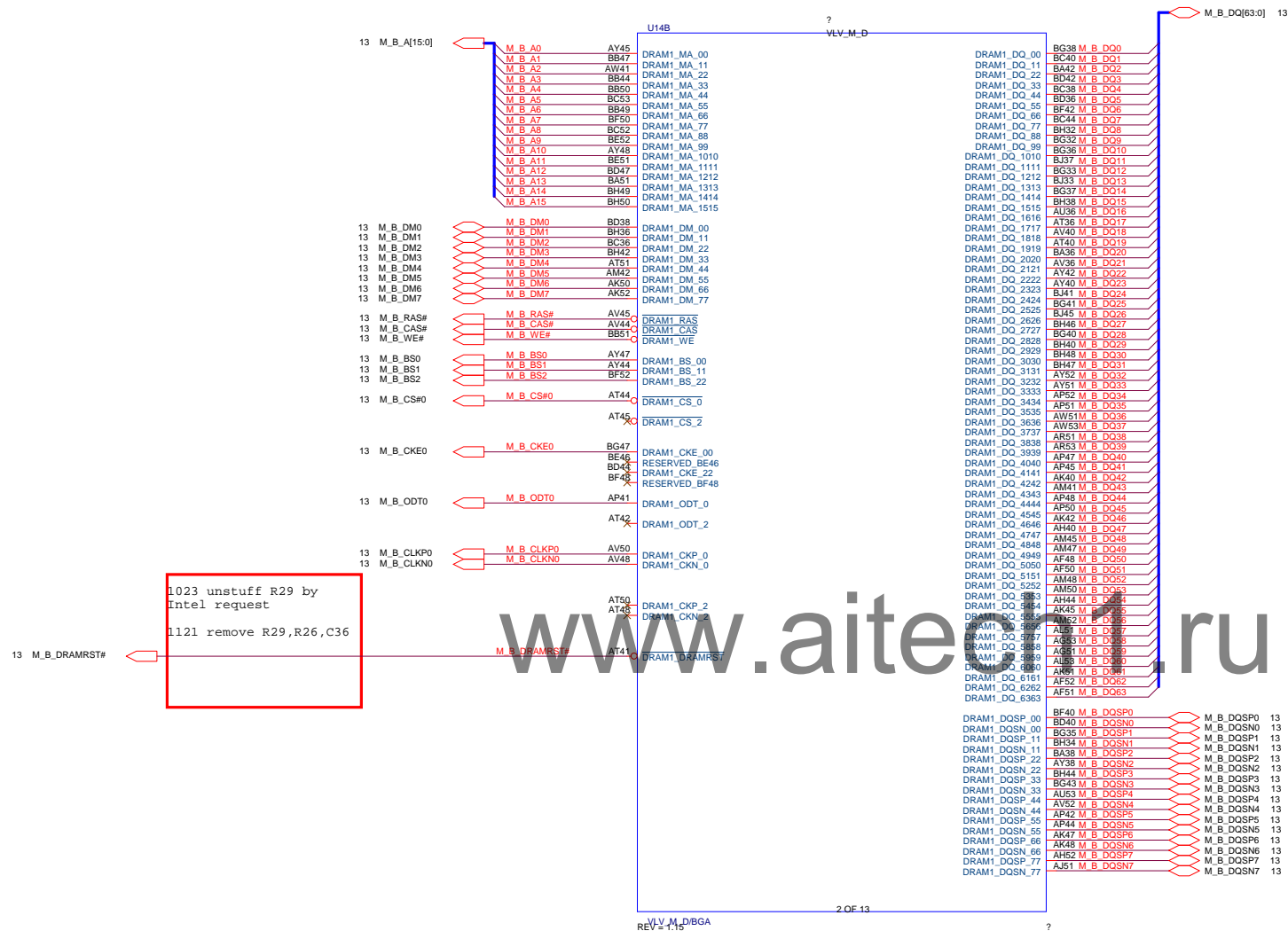
SKUA QC N2920
AJQFW3UT05--CPU (1170P)N2920 1.86G QFW3(FCBGA)
SKUB DC N2820
AJQFW4UT02--CPU (1170P)N2820 2.13G QFW4(FCBGA)





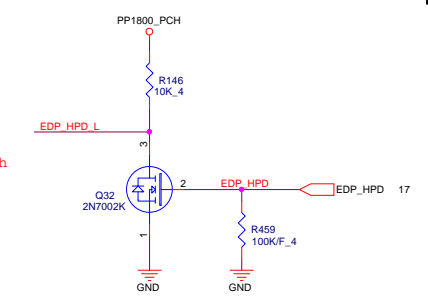
PROJECT : Peach
Quanta Computer Inc.

Size Custom	Document Number Valley 1/9 (DDR4)	Rev 1A
Date: Friday, July 25, 2014	Sheet 2 of 40	



PROJECT : Peach
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Valley 2/9 (DDRb)	1A
Date: Friday, July 25, 2014	Sheet 3 of 40	




Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is unchanged 1 = Top address bit is inverted	
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC 1 = SPI	
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override 1 = Normal operation	
DDI0_DDCDATA	DDI0 Detect	PWROK	0 = DDI0 not detected 1 = DDI0 detected	
DDI1_DDCDATA	DDI1 Detect	PWROK	0 = DDI0 not detected 1 = DDI0 detected	
GPIO_SO_NC_13				

Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is unchanged 1 = Top address bit is inverted	
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC 1 = SPI	
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override 1 = Normal operation	
DDI0_DDCDATA	DDI0 Detect	PWROK	0 = DDI0 not detected 1 = DDI0 detected	
DDI1_DDCDATA	DDI1 Detect	PWROK	0 = DDI0 not detected 1 = DDI0 detected	
GPIO_SO_NC_13				

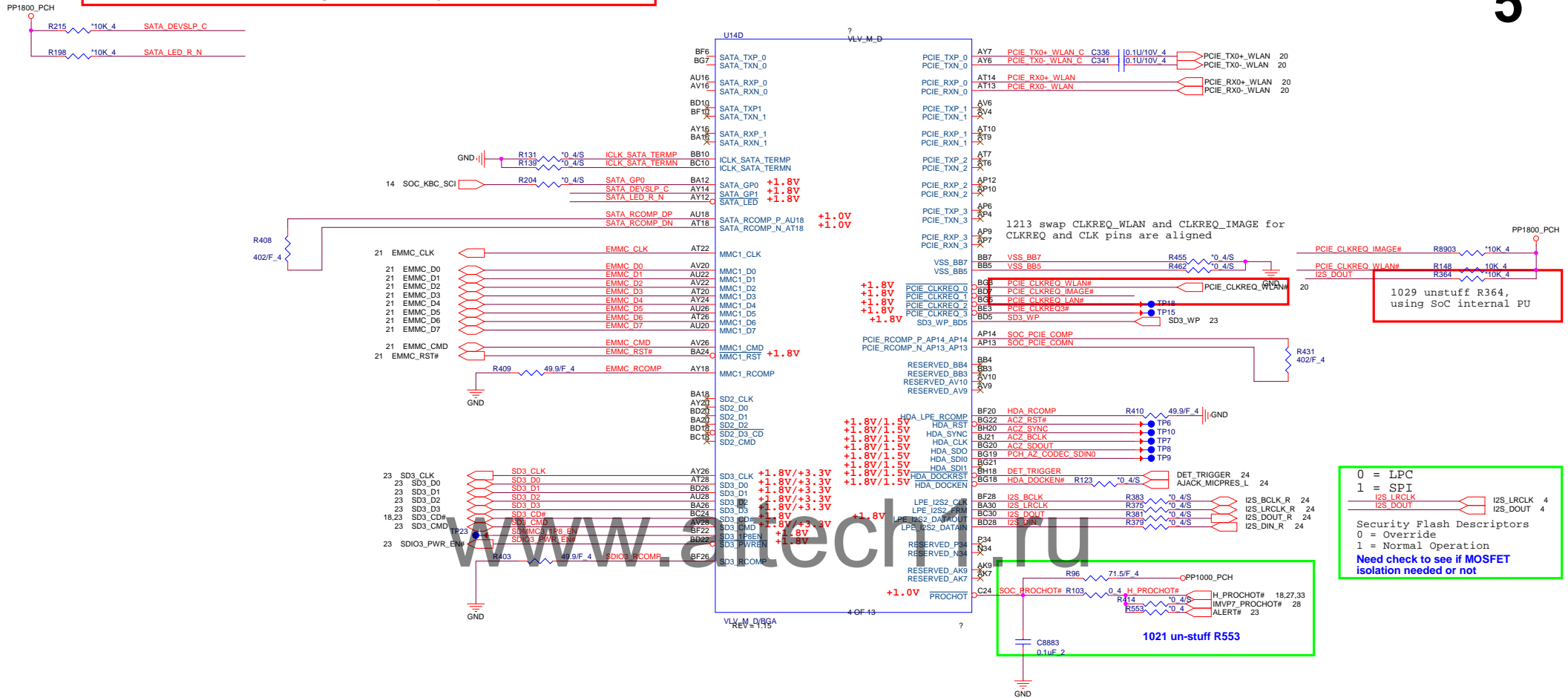
1029 unstuff R128, using SoC internal PU

1029 unstuff R372, using SoC internal PU

1115 stuff R372, system can't boot if un-stuff R372 on
proto1.5 board, need intel double confirm before proto2

 NB5 HW	PROJECT : Peach be det Quantia Computer Inc.		
	Size Custom	Document Number Valley 3/9 (Display)	Rev 1A
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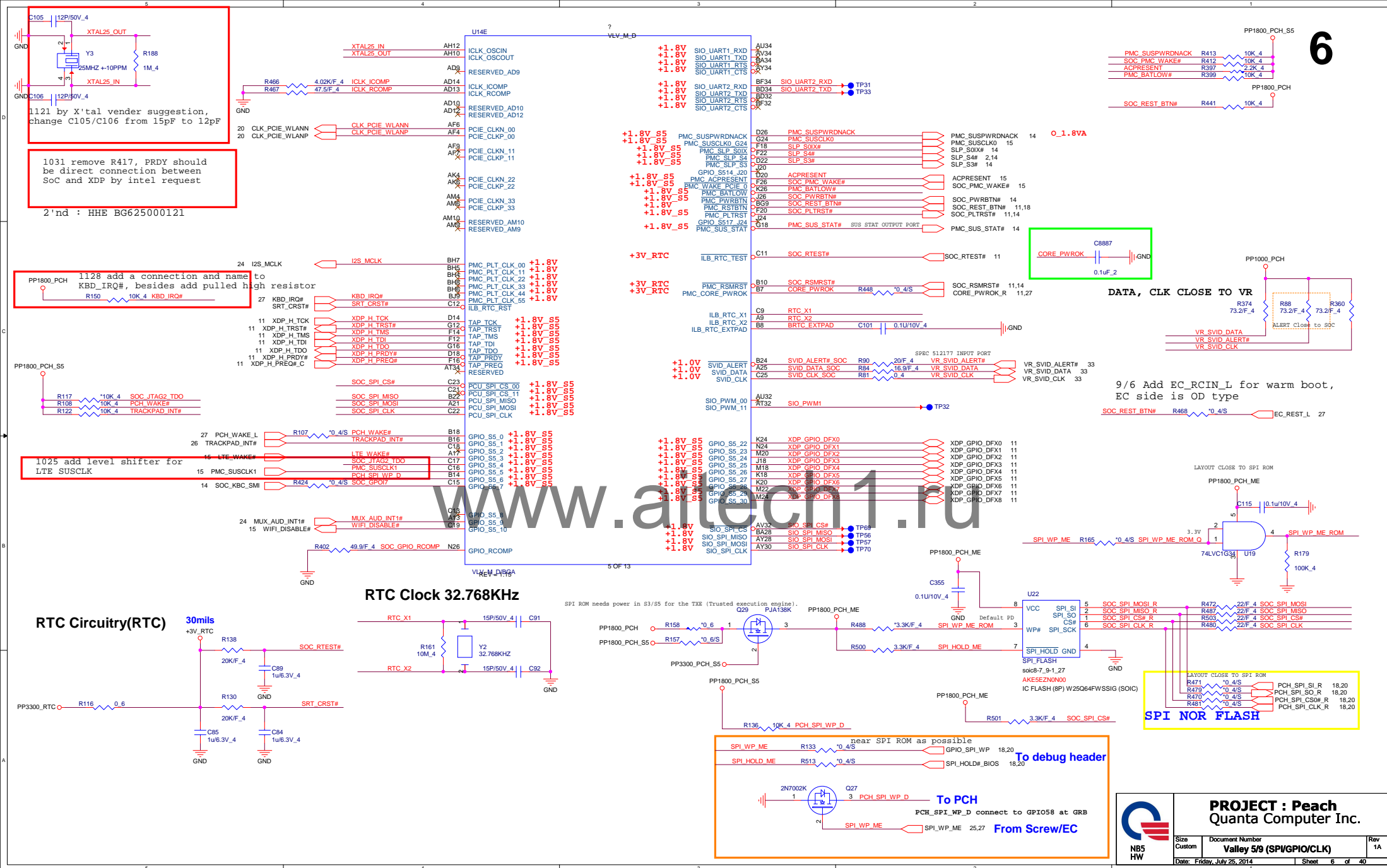
1025 Delete complete SSD(connector and caps), unstuff R215
and add test points on SATA signals

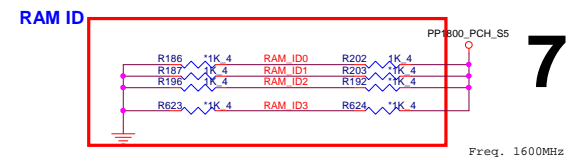


```

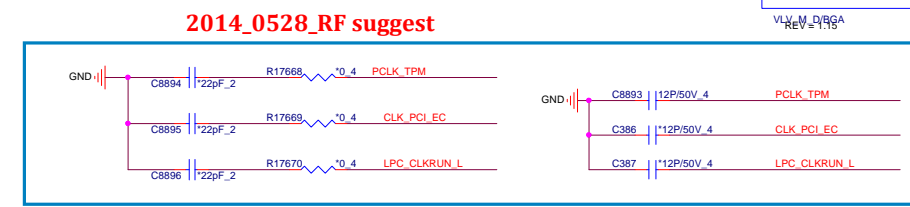
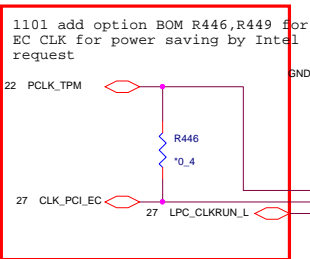
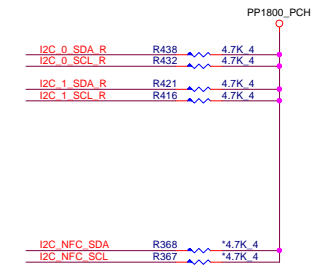
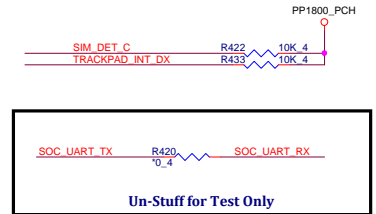
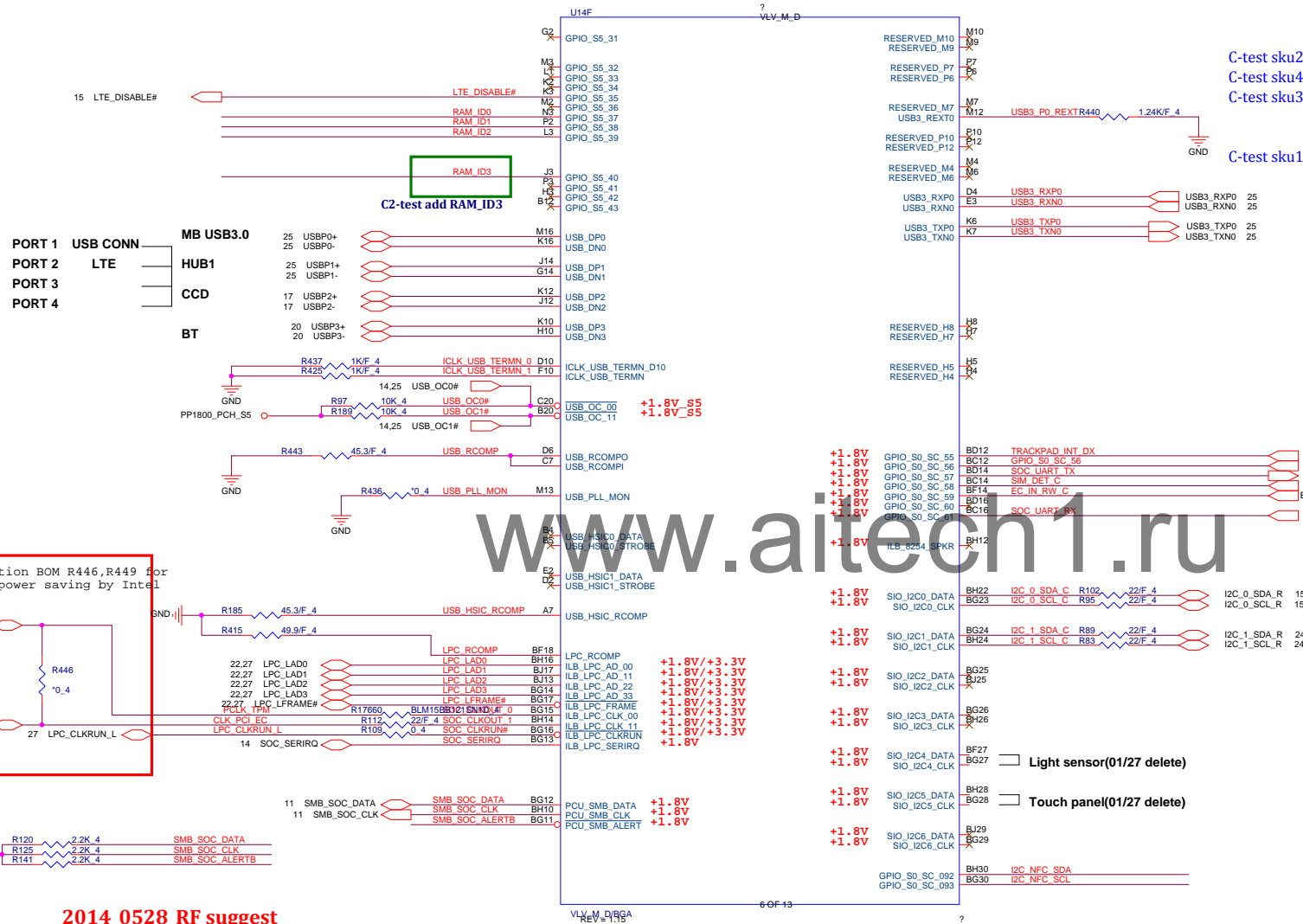
0 = LPC
1 = SPI
  I2S_LRCLK
  I2S_DOUT
  I2S_LRCLK 4
  I2S_DOUT 4
Security Flash Descriptors
0 = Override
1 = Normal Operation
Need check to see if MOSFET
isolation needed or not

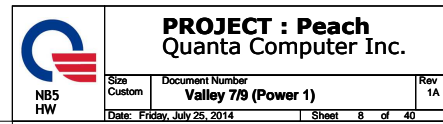
```

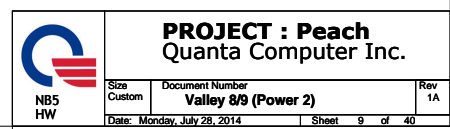




Vender	RAM_ID	Q PN	Mfr. PN	Channel	Size
Hynix	001	AKD5JGETW11	H5TC4G63AFR-PBA	2CH	4GB
Elpida	000	AKD5JGST410	EDJ4216EFBG-GNL-F	2CH	4GB
Hynix	011	AKD5JGETW14	H5TC4G63AFR-PBR	2CH	4GB
Micron	010	AKD5DGSTL07	MT41K128M16JT-125M:K	2CH	2GB
Elpida	100	AKD5JGST410	EDJ4216EFBG-GNL-F	1CH	2GB
Hynix	101	AKD5JGETW11	H5TC4G63AFR-PBA	1CH	2GB
Hynix	110	AKD5JGETW14	H5TC4G63AFR-PBR	1CH	2GB







<DDR>

BYTE2_16-23

BYTE1_8-15

BYTE0_0-7

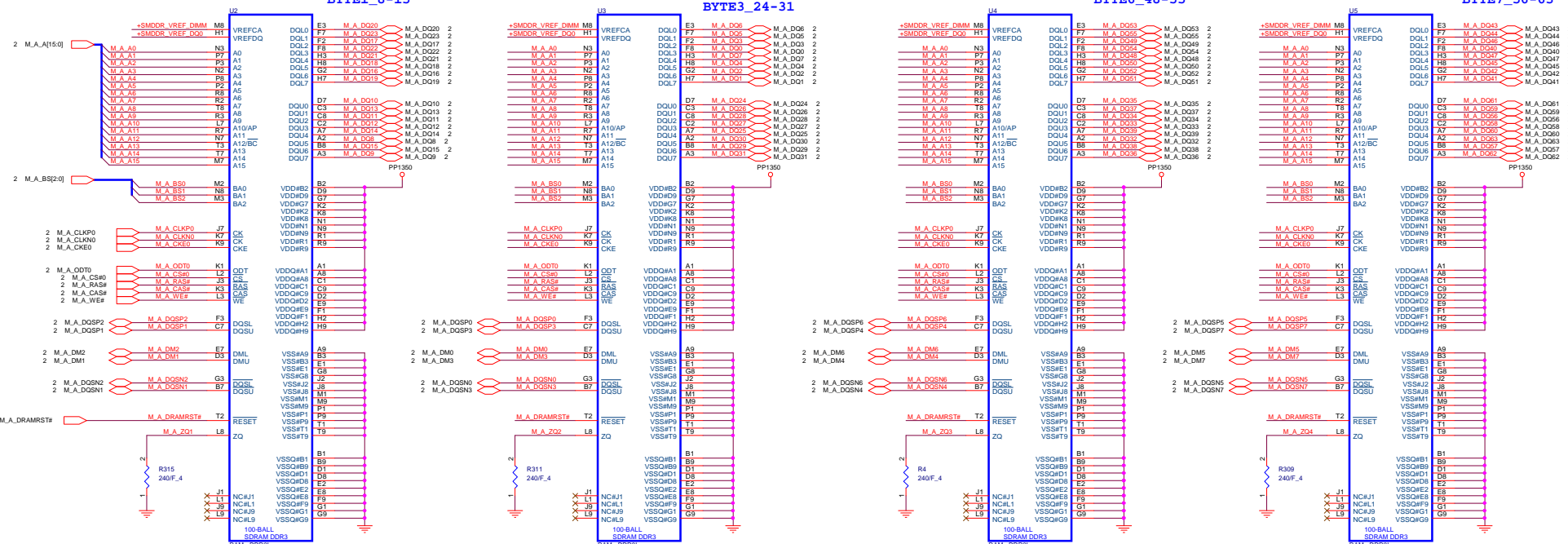
BYTE3_24-31

BYTE4_32-39

BYTE6_48-55

BYTE5_40-47

BYTE7_56-63



Vendor	P/N	
Hynix		
Elpida		
	AKD5JGST400	DDR3L 1333MHz 4gb
	AKD5JGST404	DDR3L 1600MHz 4gb

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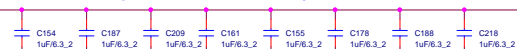
1024 change ODT PU to VTT by Intel request

1023 change cap from 0.2pF to 3.3pF

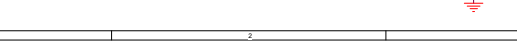
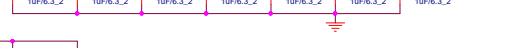
Distributed around all DRAM devices (CHA and CHB)



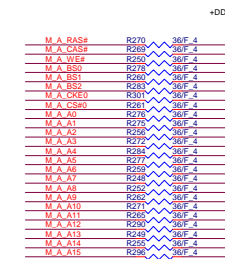
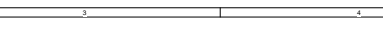
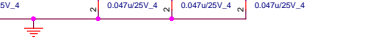
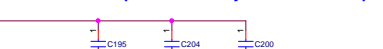
Place these Caps near each X16 Memory Down



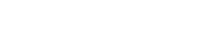
1205 add 0.1uFx2 on PP1350 for EMI request



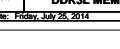
Place these Caps near Memory Down CA & DQ pin



M1 solution



M1 solution



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Quanta Computer Inc.

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ment Number
DDR3L MEMORY DOWNx16 A
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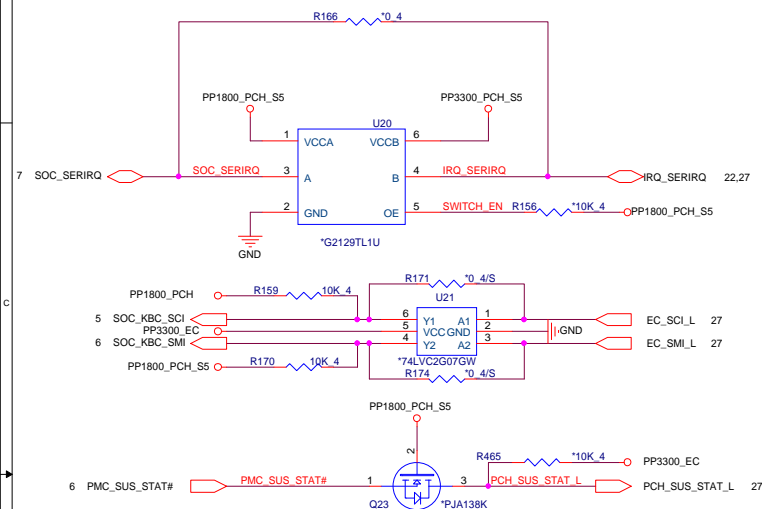
DATE: 10-15

BTES-10-17

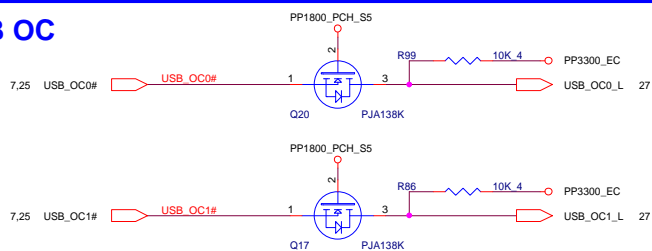


PWRON SEQUENCE

```
9/6 EC table says SERIRQ is OD pin, reserve for debugging
1128 remove R166, because SERIQR of TPM needs 3V
1128 reserve 0 ohm R387/R391 on VCCA and VCCB for debugging
```

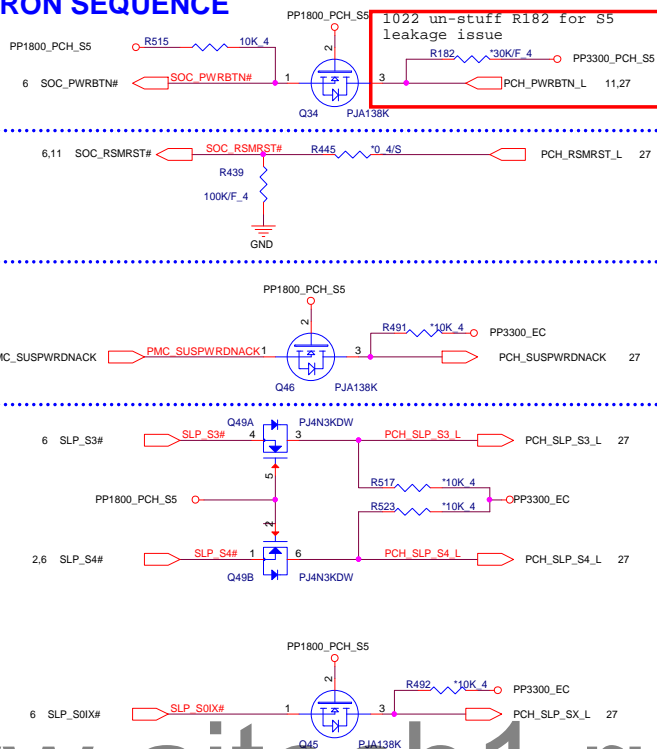


USB OC

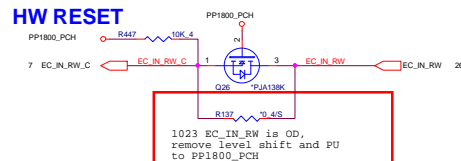
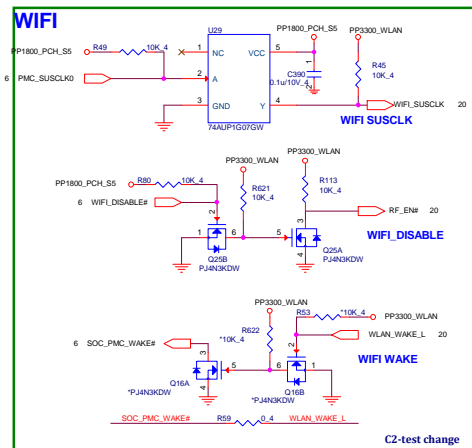
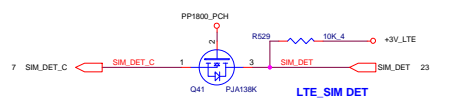
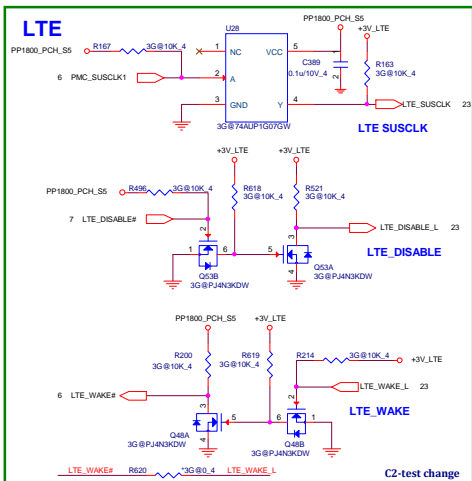


Stuffing for notifying EC

PWRON SEQUENCE



0220 remove SPI_SIO Interface,
Q35,Q36,Q37,Q44,R486,R484,R485,
R483,R426,R429,R427,R428



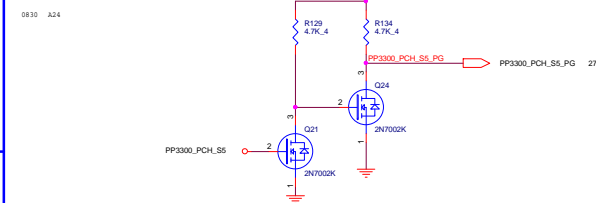
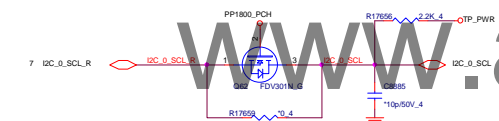
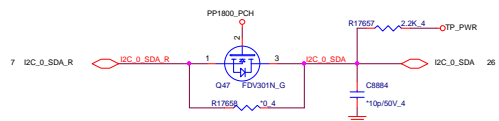
Touch Screen(01/27 delete)

S0

S5

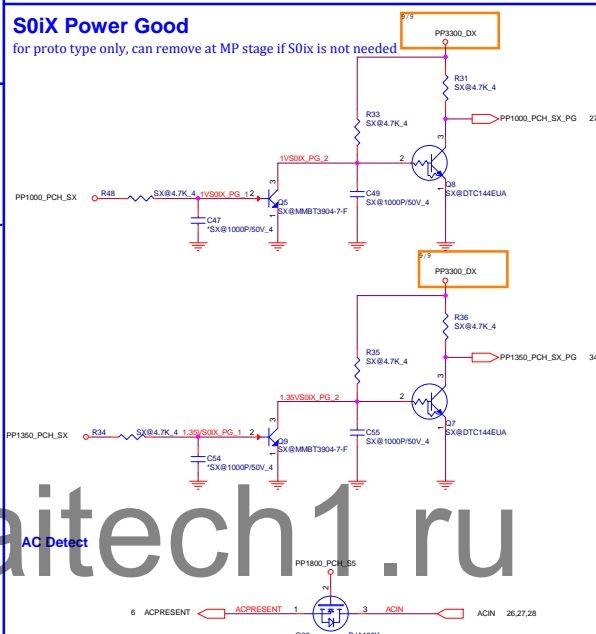
SATA

1025 Delete complete SSD(connector and caps)

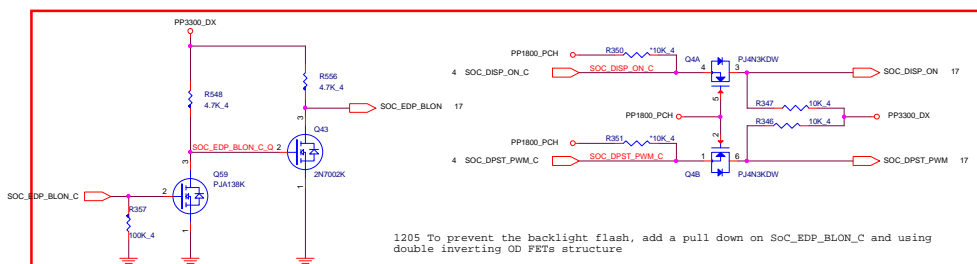


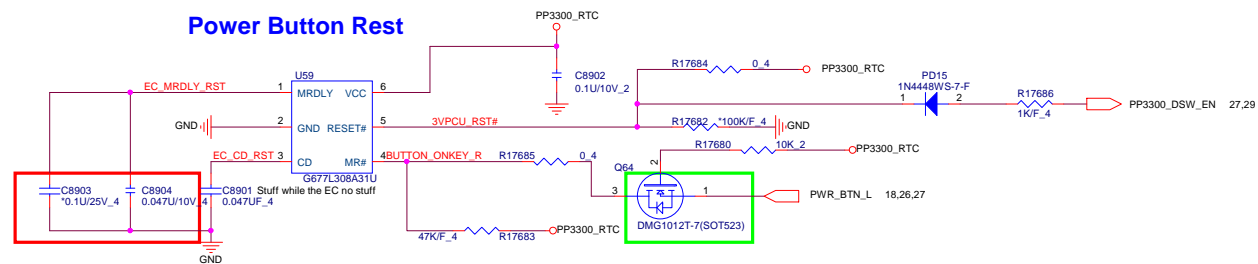
S0iX Power Good

for proto type only, can remove at MP stage if S0ix is not needed



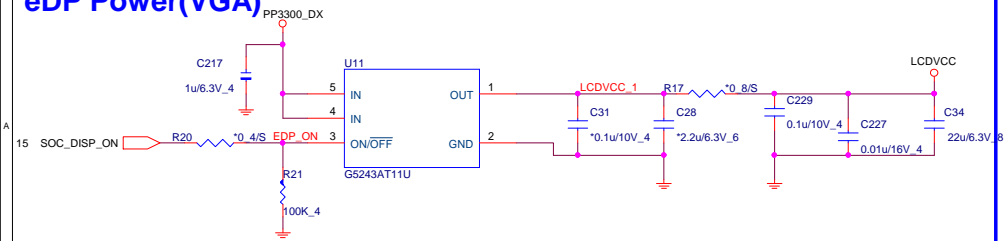
AC Detect



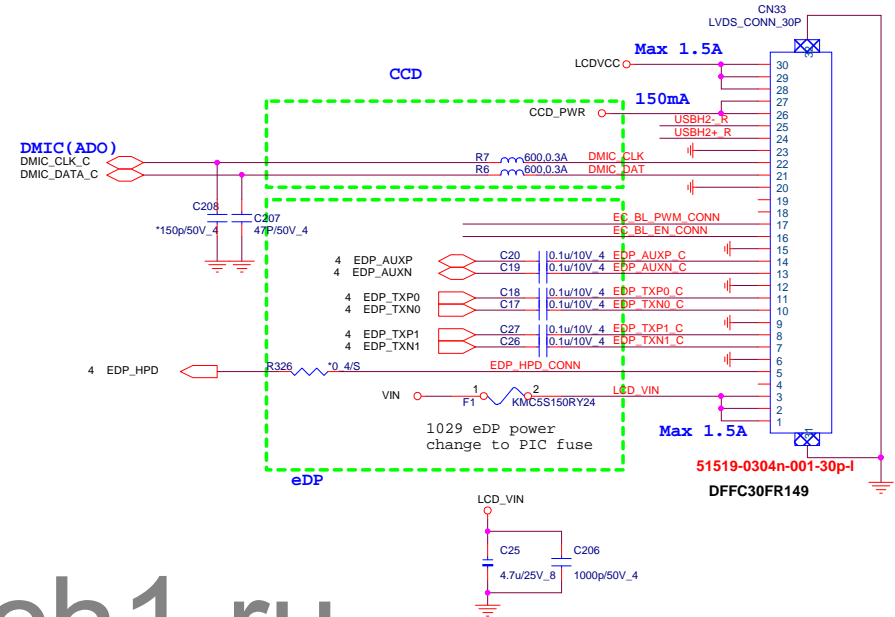


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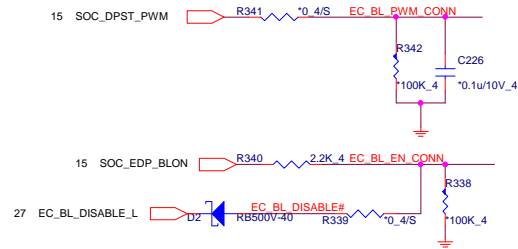
eDP Power(VGA)



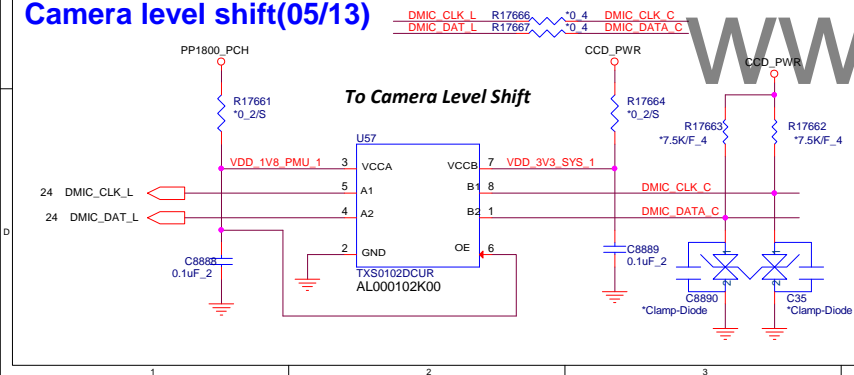
eDP(VGA)



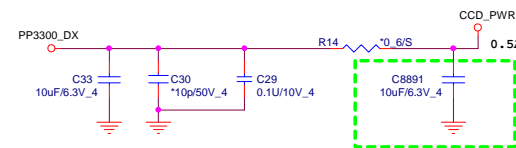
eDP panel control(VGA)



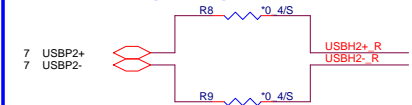
Camera level shift(05/13)



CCD power(CCD)



CCD USB(CCD)



PROJECT : Peach
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EDP/CCD/DMIC/TS	1A
Date: Friday, July 25, 2014	Sheet 17 of 40	

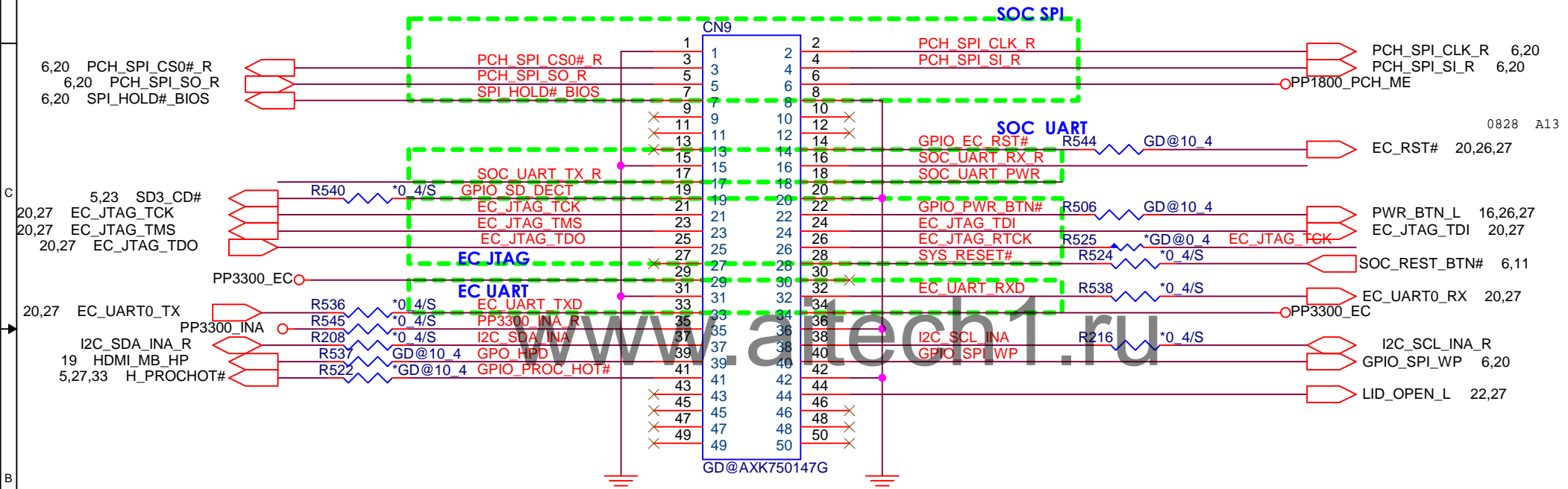
GOOGLE Debug Port(MPC)

50 pin BTB is MUST, don't use 42 pin

Socket part number AXK750147G

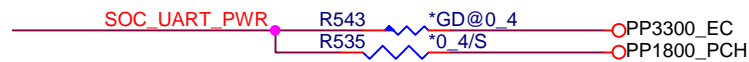
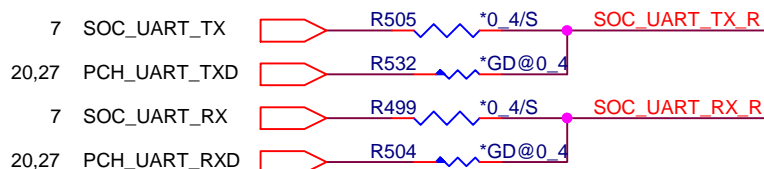
PIN7 OD	PIN39 OD	PIN49 OD
PIN14 OD	PIN41 OD	PIN50 OD
PIN19 OD	PIN43 OD	
PIN22 OD	PIN44 OD	
PIN28 OD	PIN45 OD	
PIN30 OD	PIN46 OD	
PIN37 OD	PIN47 OD	
PIN38 OD	PIN48 OD	

18



1021 change footprint and PN

9/13 add pull up



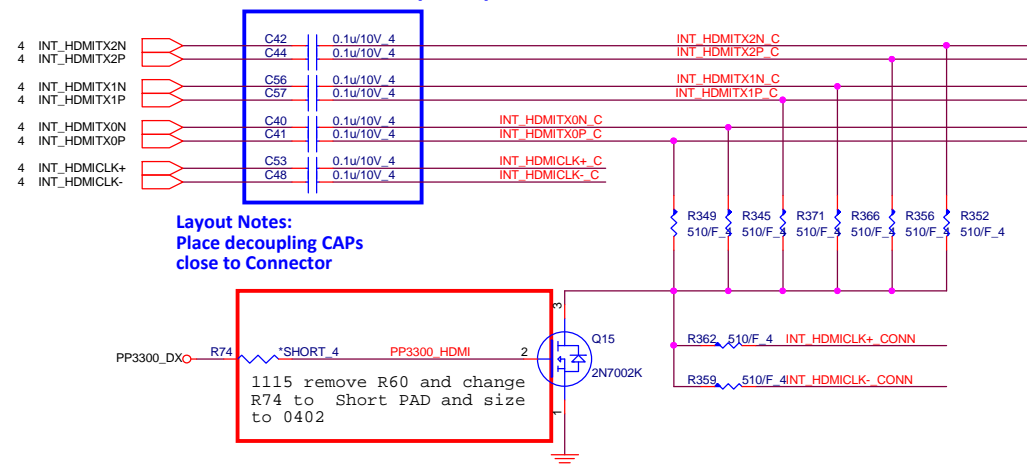
9/6 using optional instead of level shifted, default is from SoC



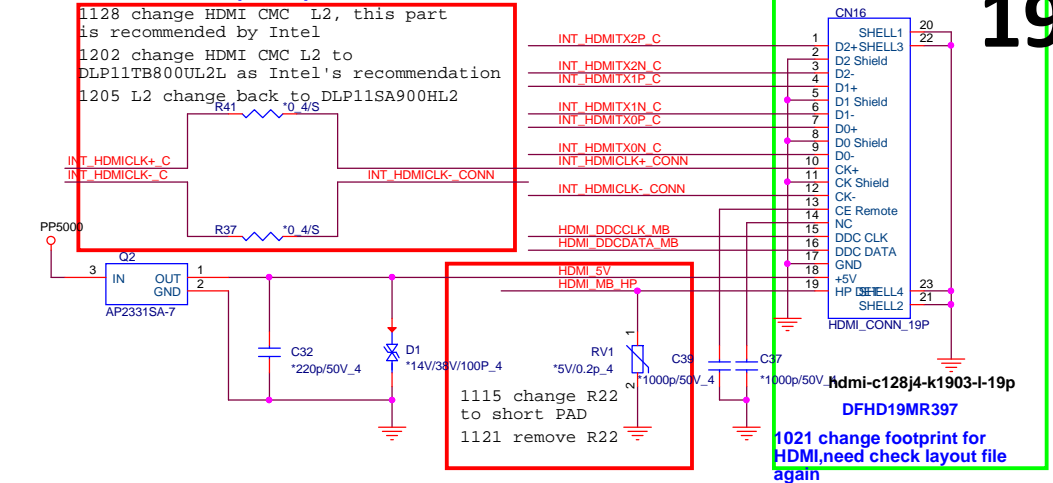
PROJECT : Peach
Quanta Computer Inc.

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HDMI Cost Reduced level shift (HDM)

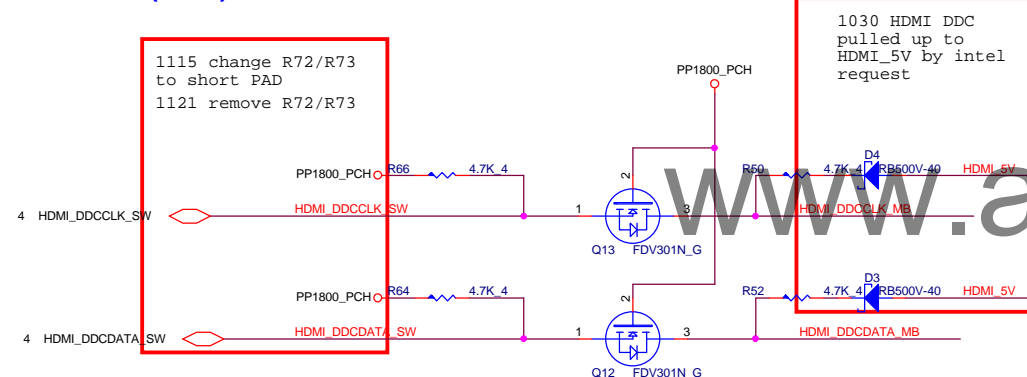


HDMI connector (HDM)

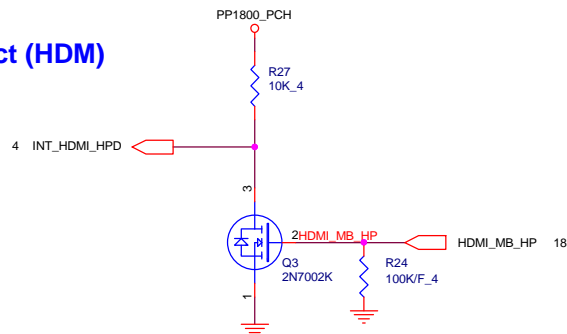


19

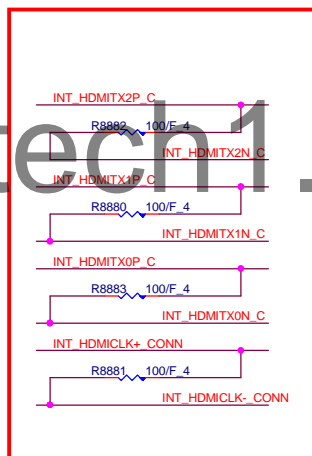
HDMI DDC (HDM)



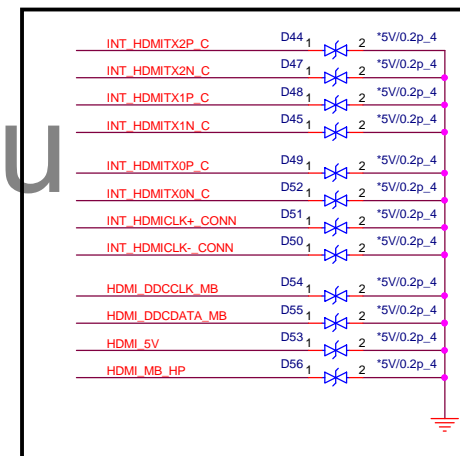
HDMI-detect (HDM)



EMI

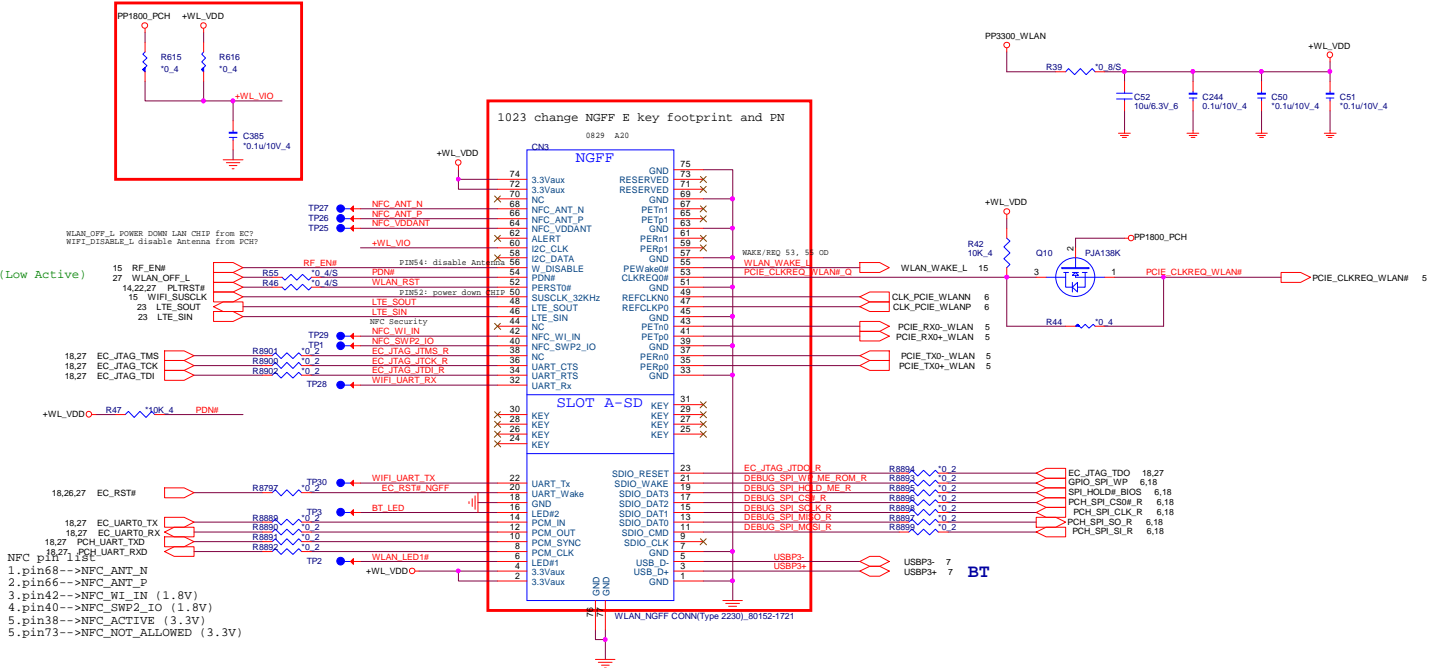


ESD 靠近HDMI CONNECTOR(CN16)



PROJECT : Peach
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Custom	HDMI	1A
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LTE Coexistence pin list (based on V0.2 spec)

- 1.pin48-->LTE_SOUT (3.3V)
- 2.pin46-->LTE_SIN (3.3V)

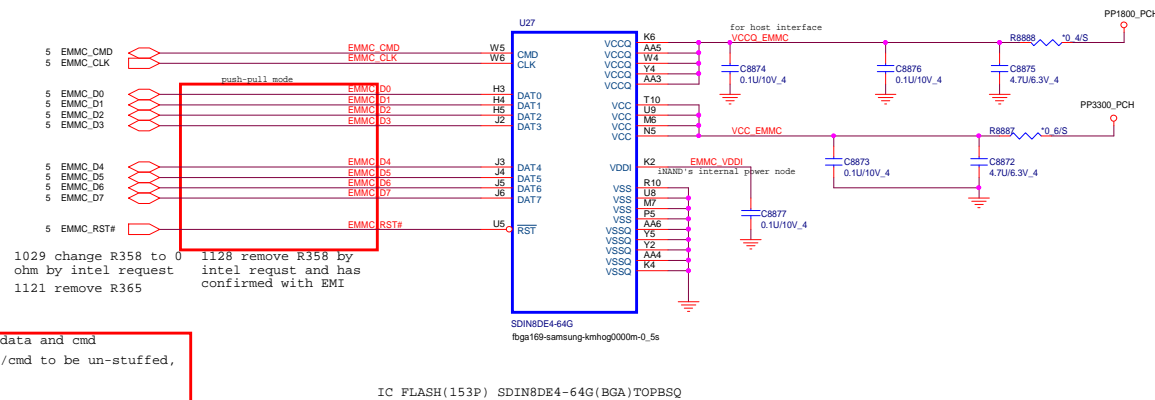
Video Codec (M.2 LGA 1216-S3) (VGA)
(0213 delete VP8/VP9)

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1025 Delete complete SSD(connector and caps)

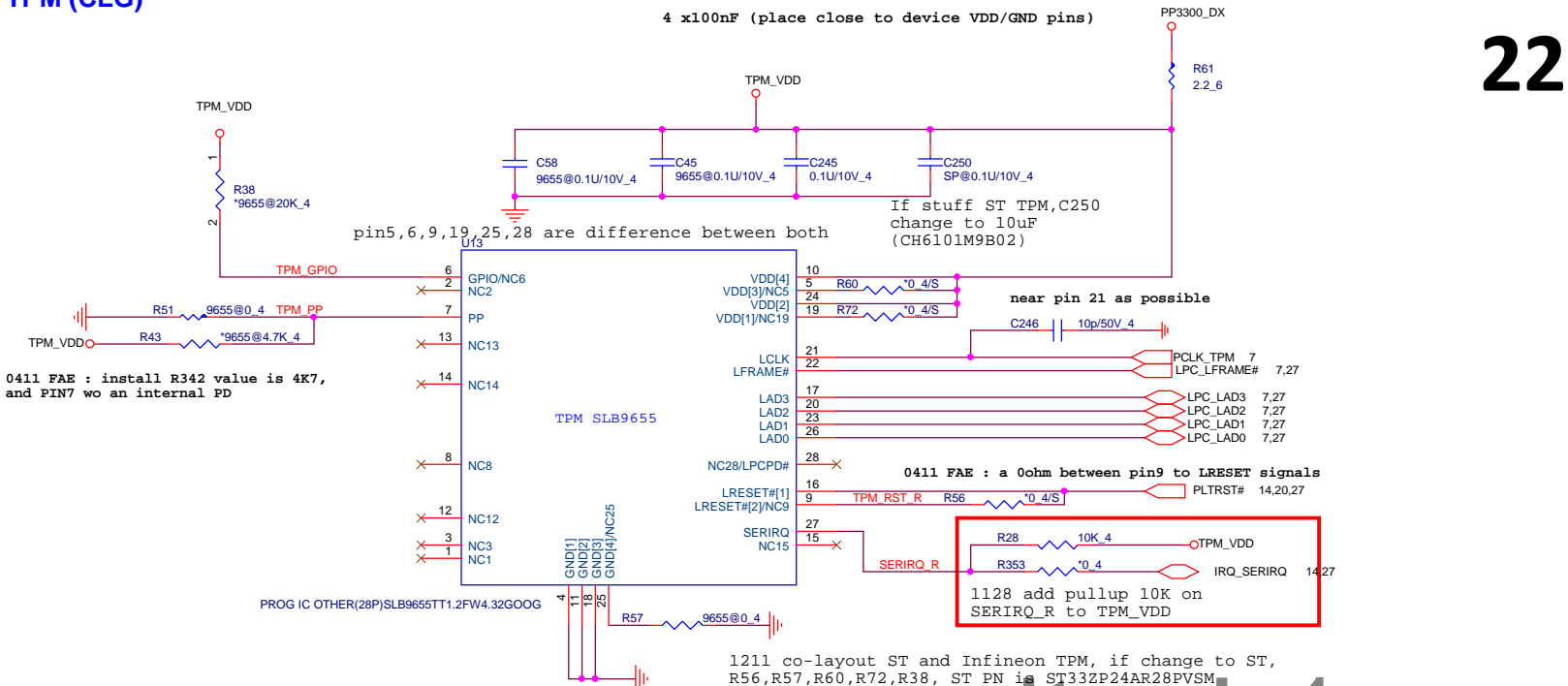
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EMMC (CBS)



R396	47K 4	EMMC D0
R401	47K 4	EMMC D1
R409	47K 4	EMMC D2
R393	47K 4	EMMC D3
R406	47K 4	EMMC D4
R405	47K 4	EMMC D5
R404	47K 4	EMMC D6
R417	47K 4	EMMC D7
R361	47K 4	EMMC CMD

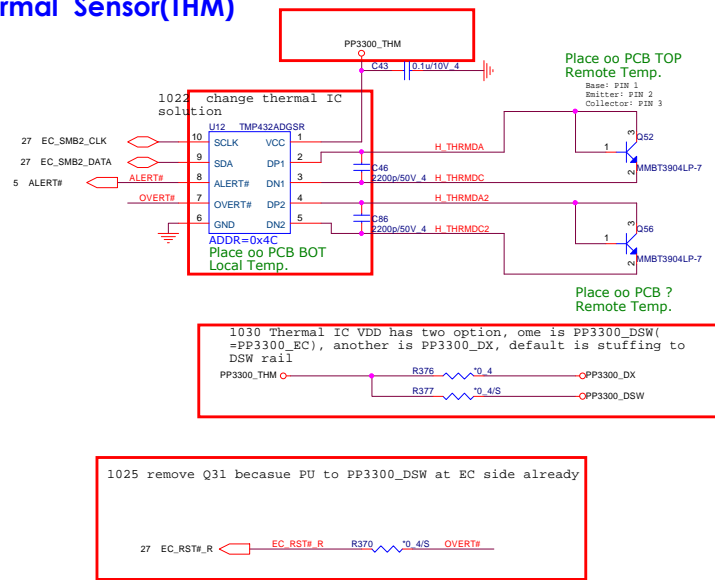
TPM (CLG)



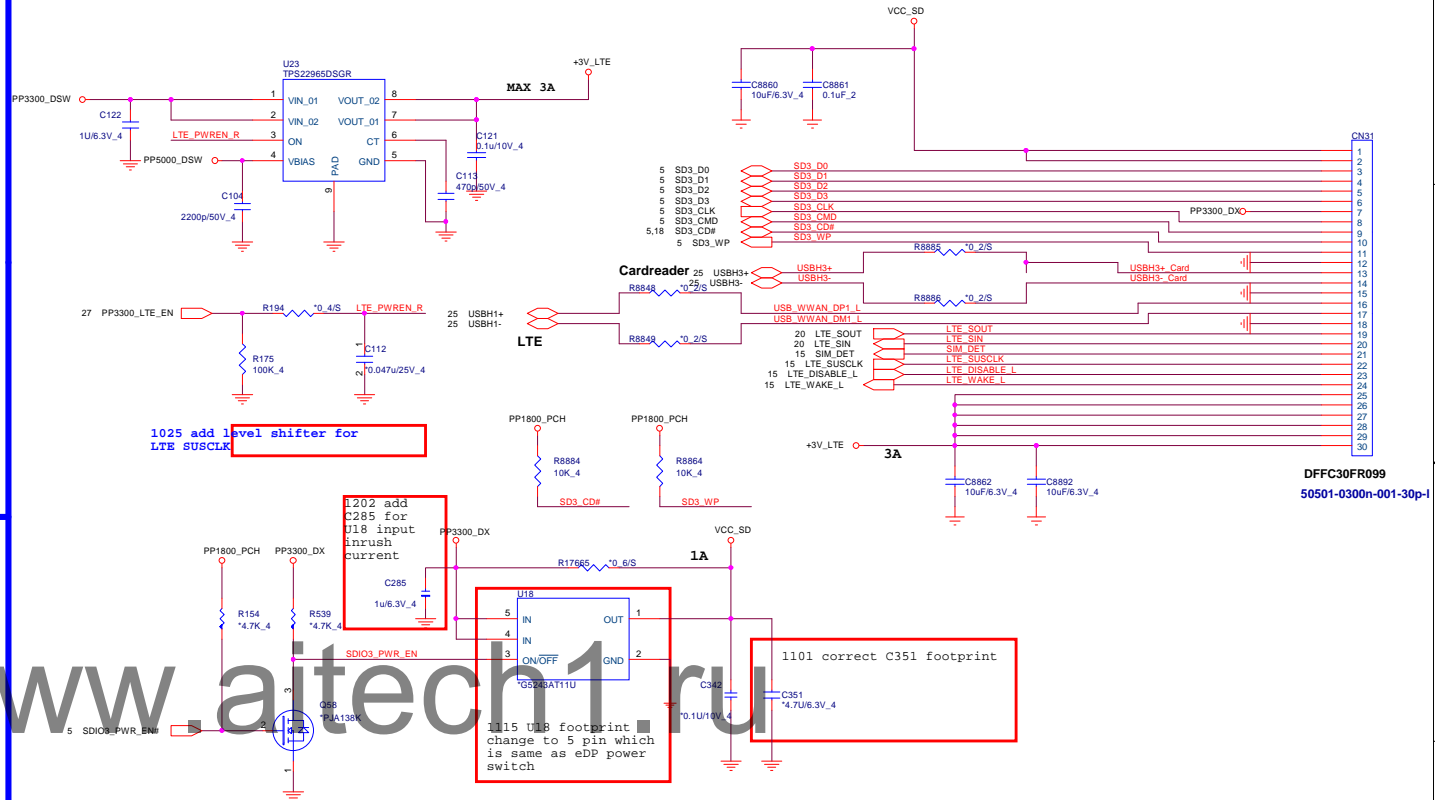
LED(UIF)



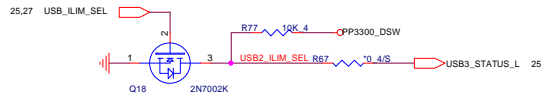
Thermal Sensor(THM)

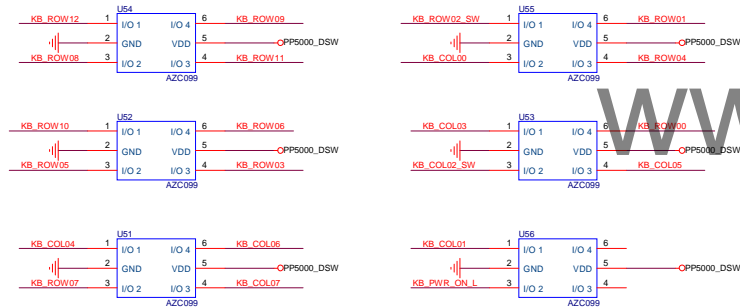
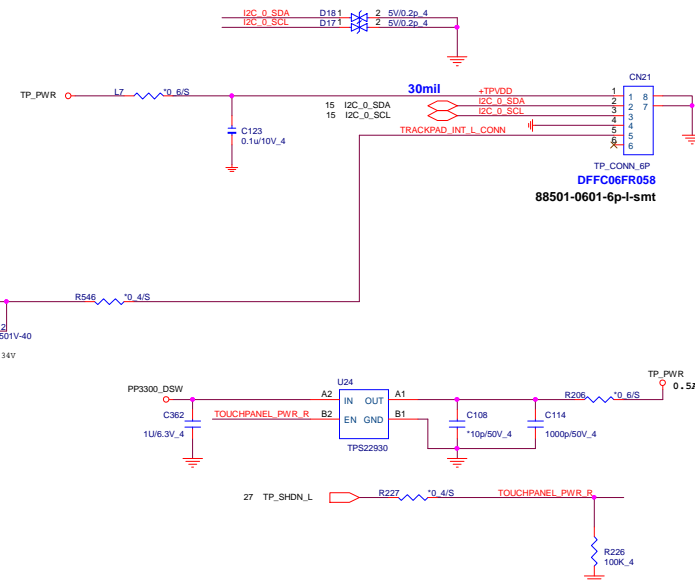


FUNCTION DB
LTE(MNC)



USB Switch Current Control



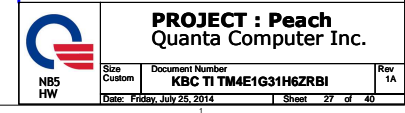


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[illegible]

- Connect to EC reset pin
- Connect to GPIO on CPU with PU to GPIO power well
- Connect to EC pin C5 (must be low when EC IN RESET)

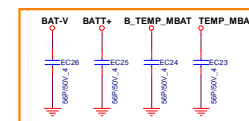
```
co-layout 4K4108 and 4K4137
SLG4K4108 (AL004108000)
SLG4K4137 (AL004137000)
4K4137 PIN3 is BATT_ENABLE
4K4137 PIN4 is AC_PRESENT
```



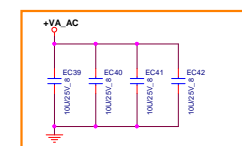


	2-cell	3-cell
PR27	un-stuff	stuff

10ms one-shot circuit

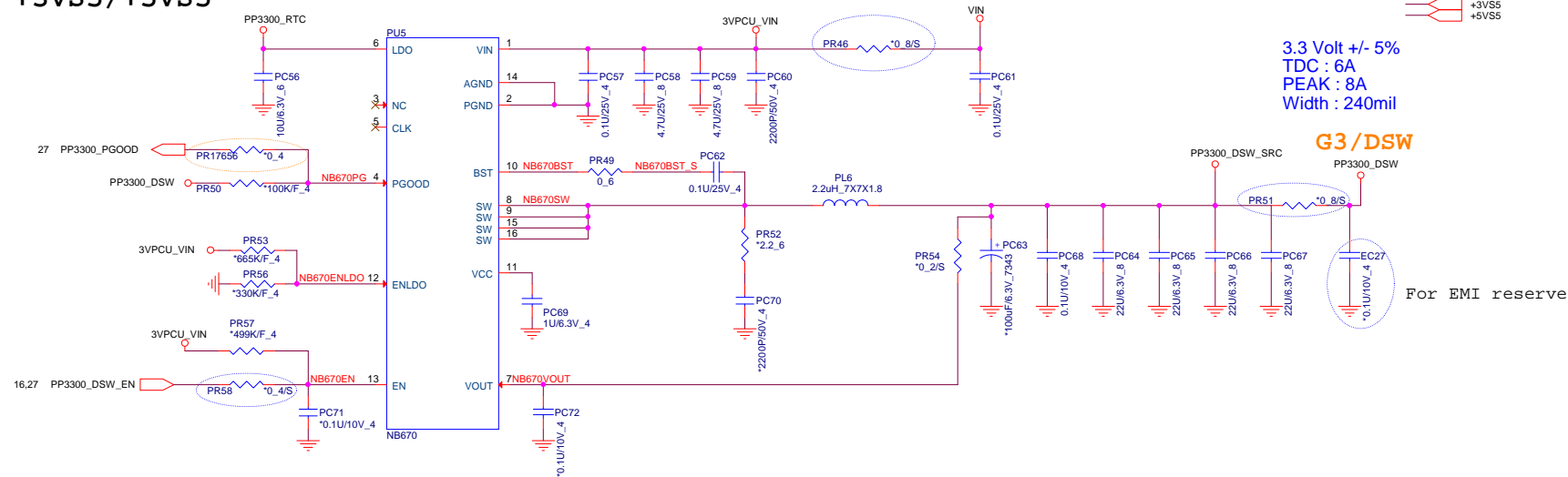


For EMI

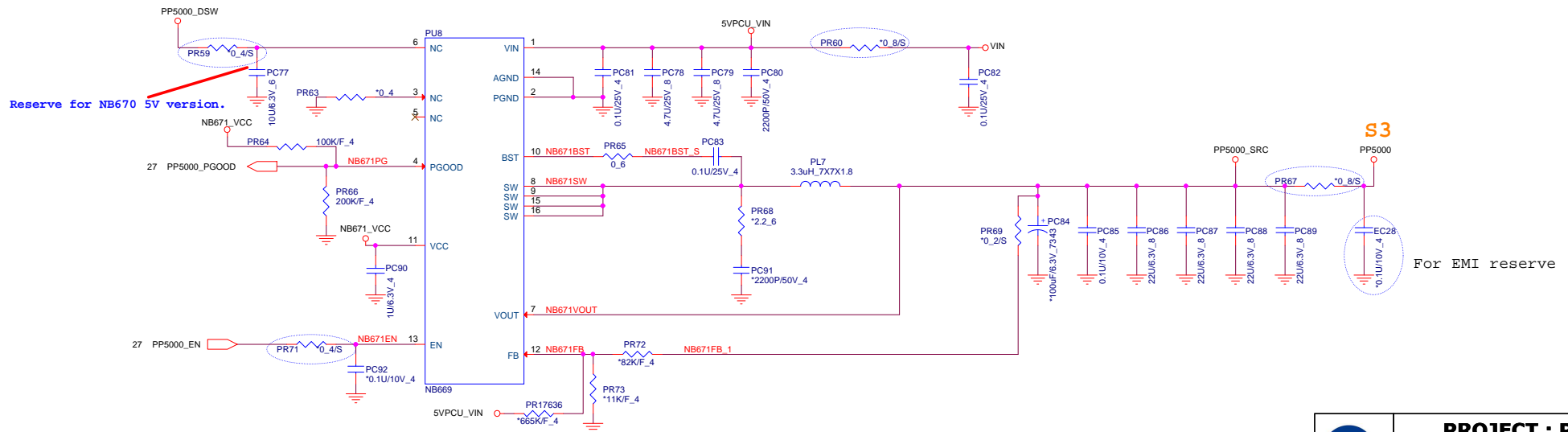


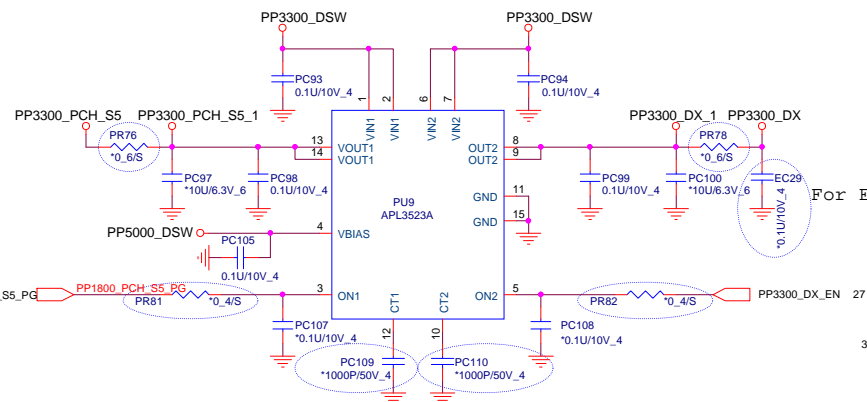
For EMI :

DC/DC +3VS5/+5VS5

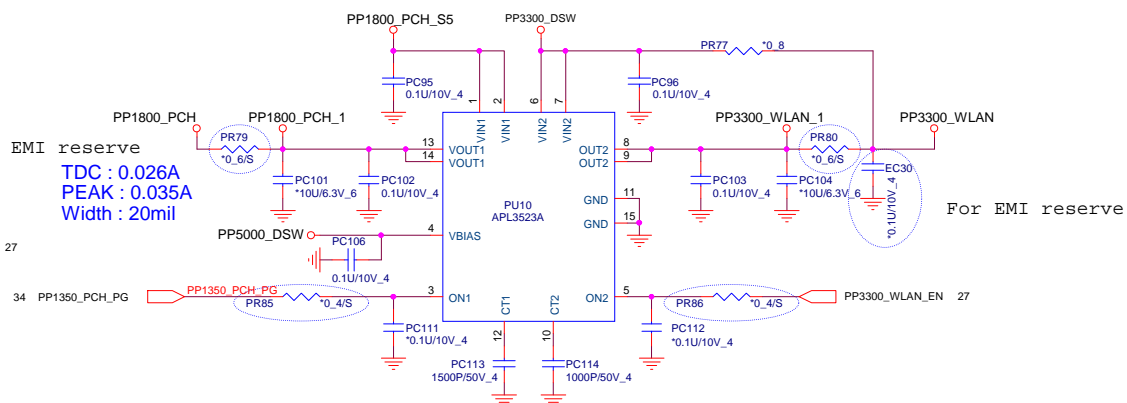


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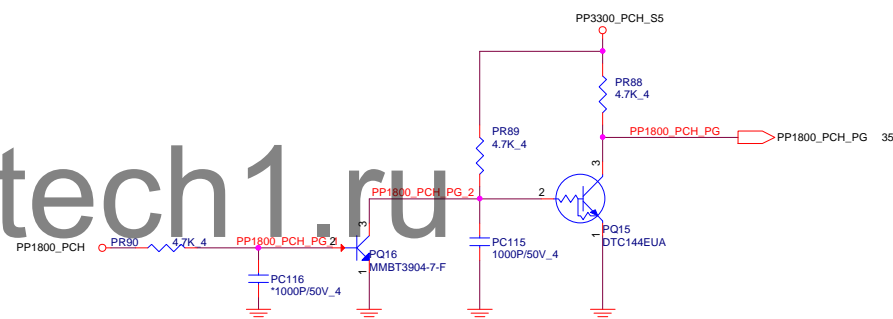


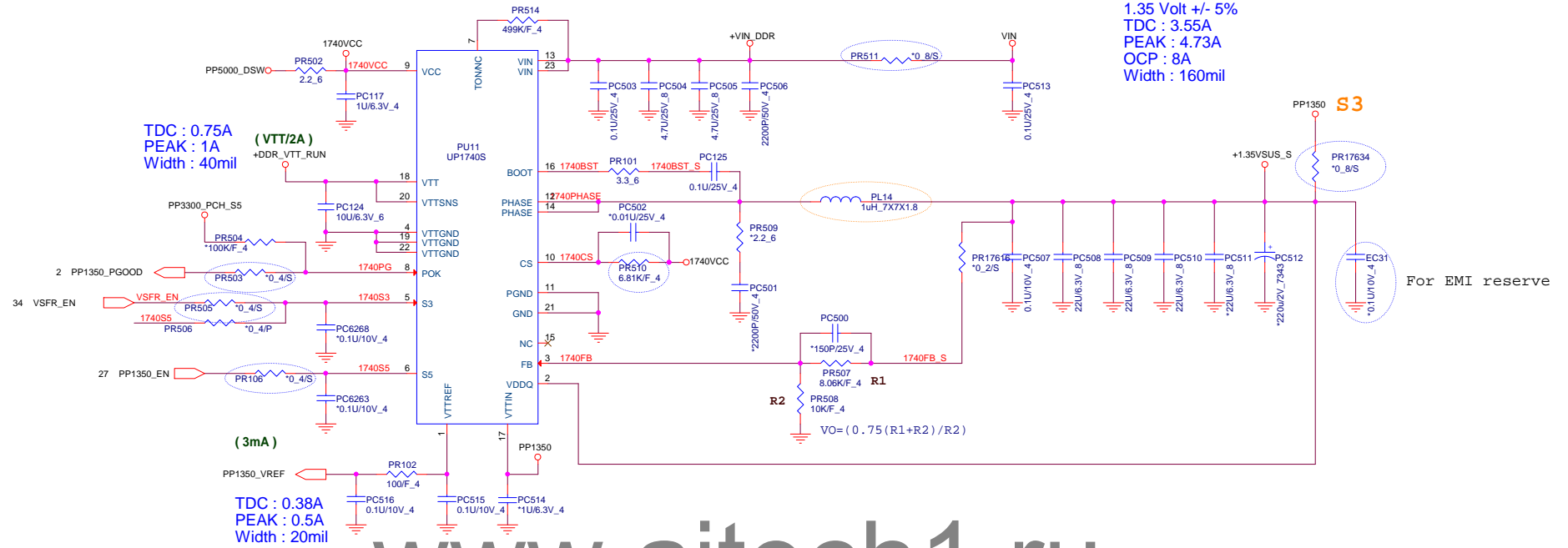


For EMI reserve
TDC : 0.026A
PEAK : 0.035A
Width : 20mil



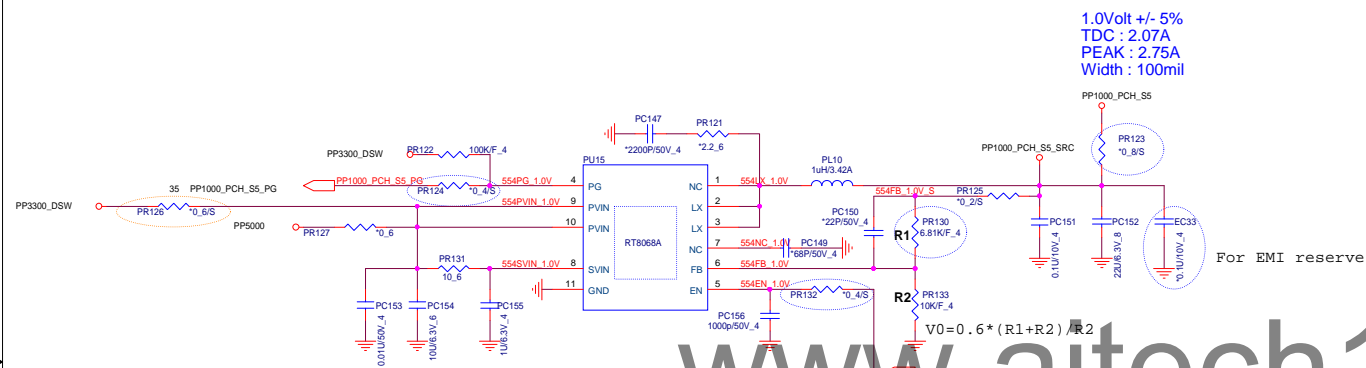
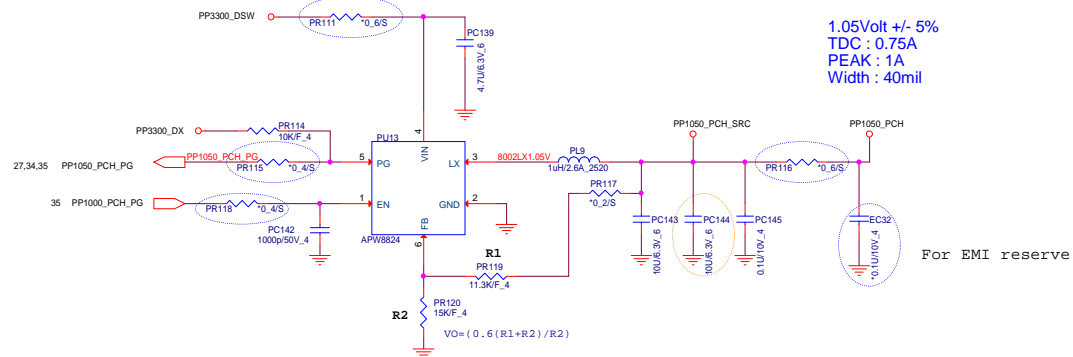
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	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (main on off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

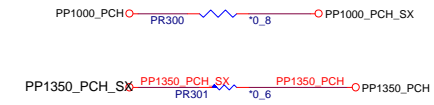


PC156
1000p/50V_4

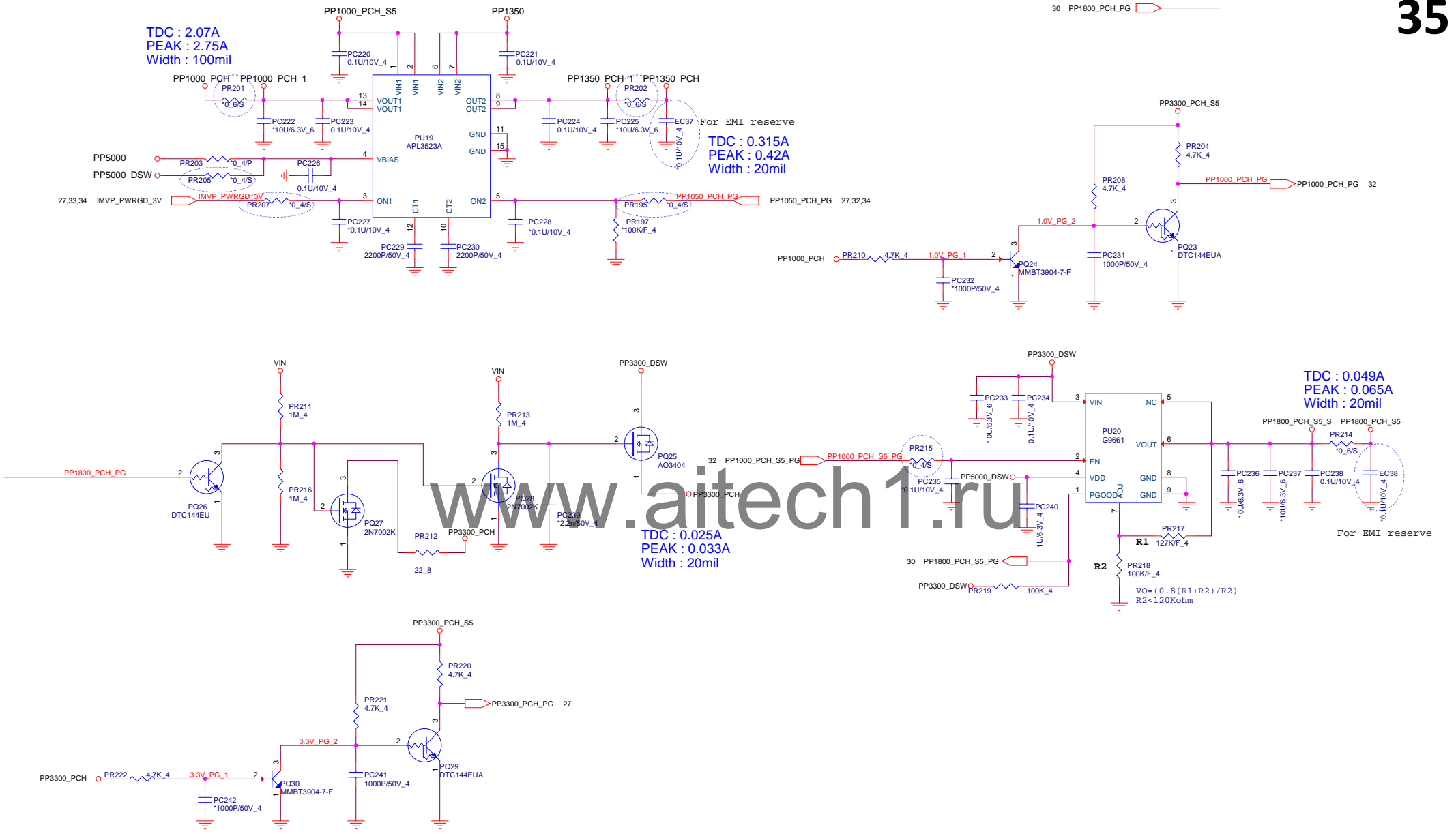
V0 = 0.6 * (R1+R2) / R2

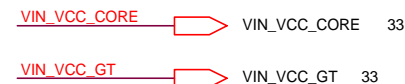
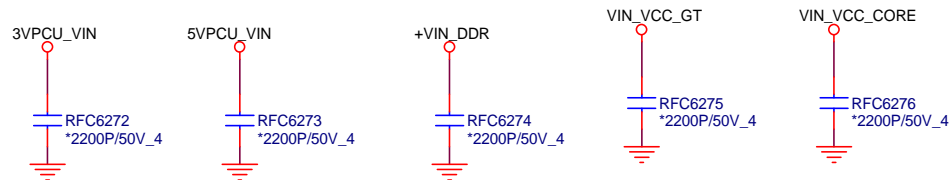
SUSP_VR_EN 27





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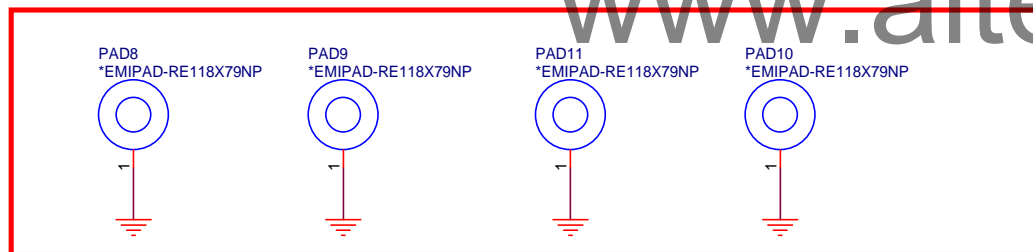




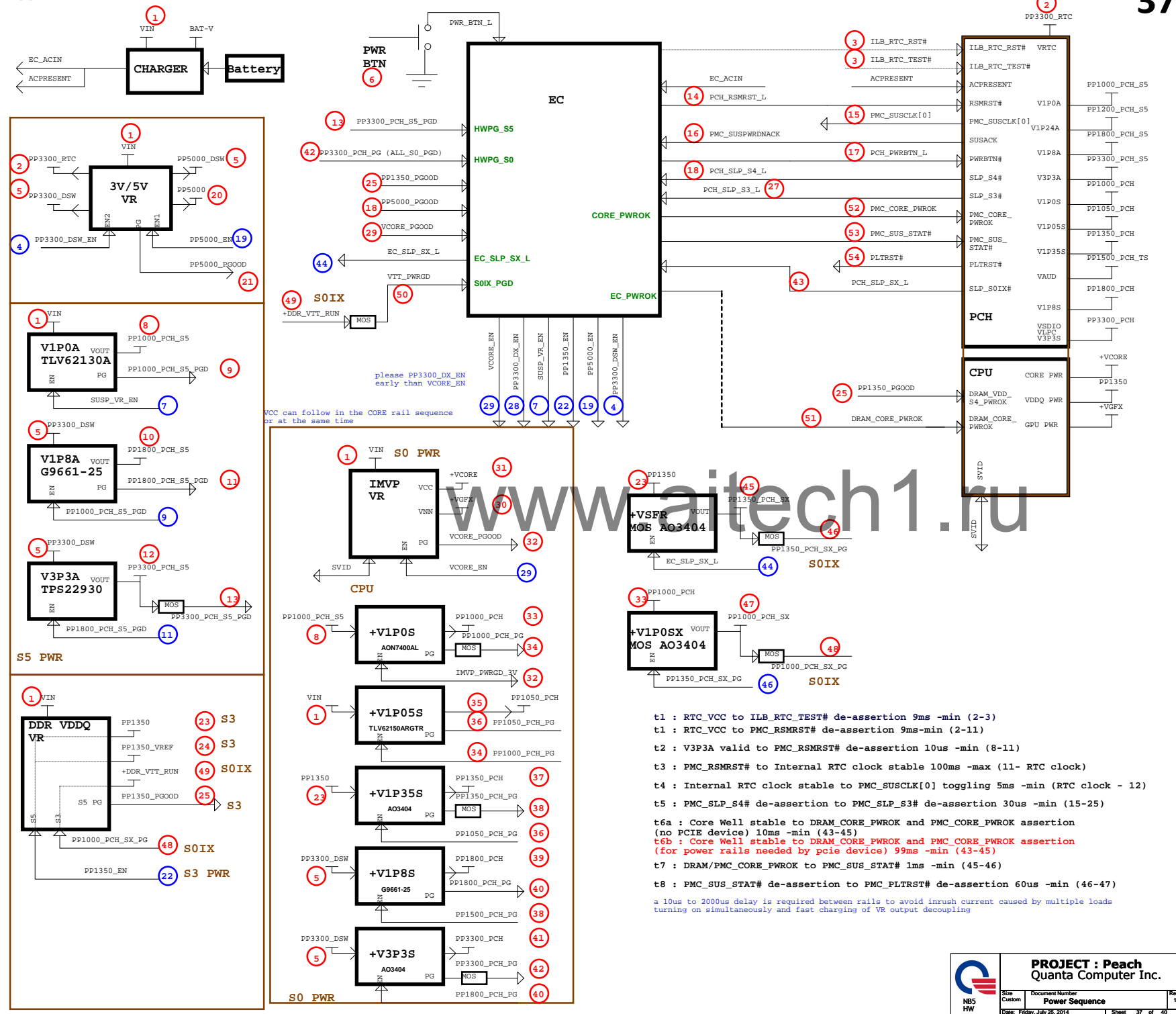
TOP



BOTTOM

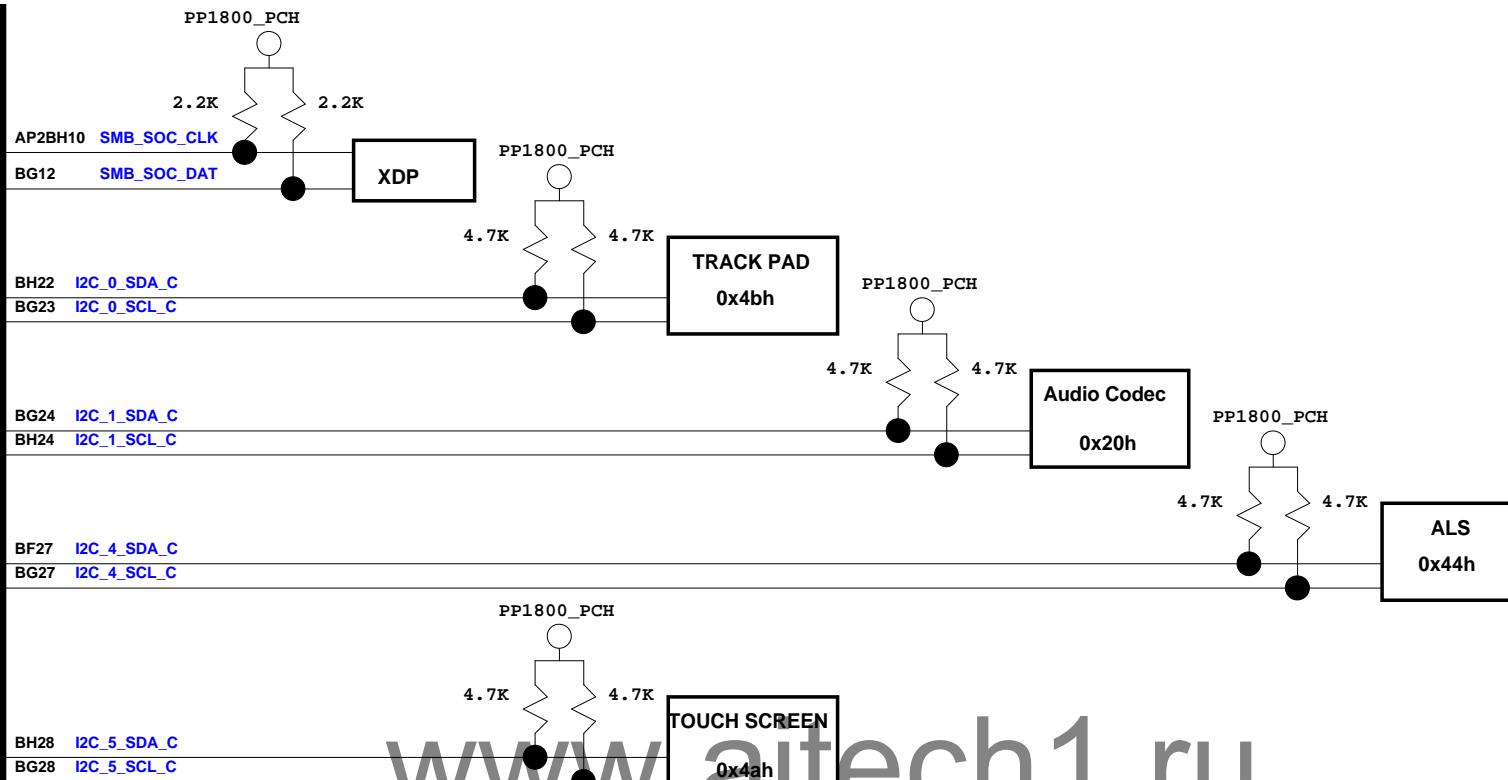


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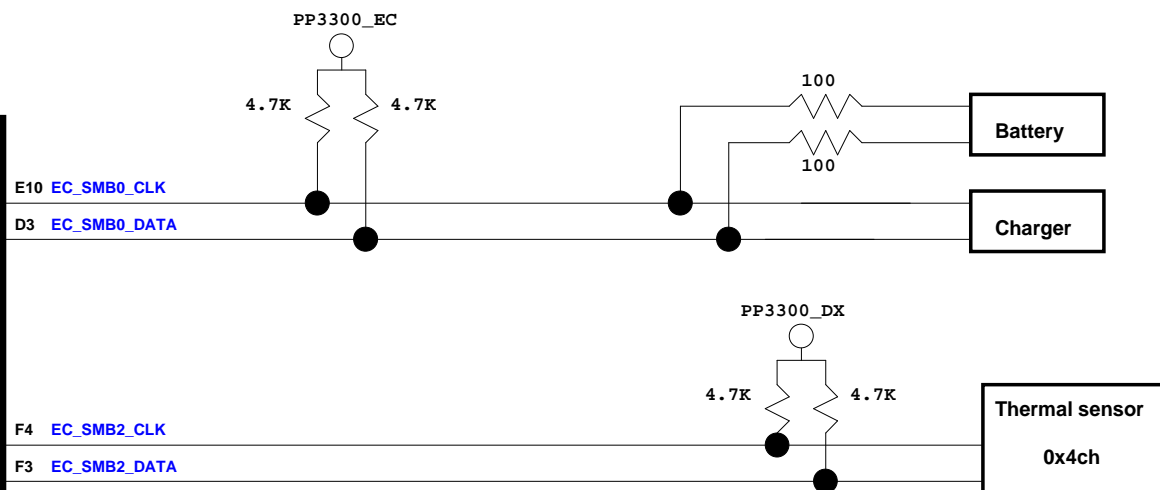


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